

MM54HC05/MM74HC05 Hex Inverter (Open Drain)

General Description

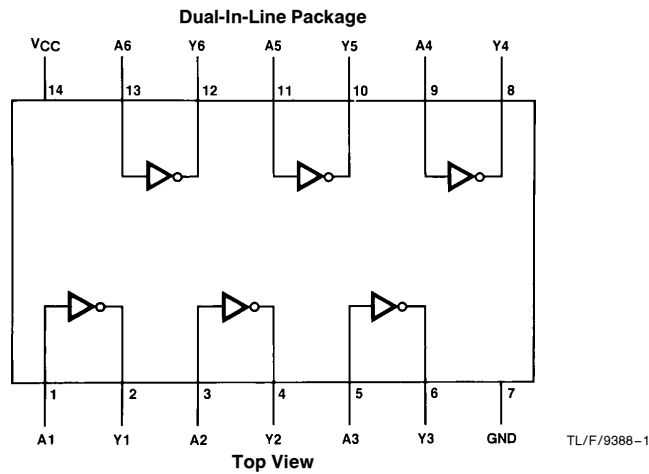
The MM54HC05/MM74HC05 are logic functions fabricated by using advanced silicon-gate CMOS technology, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are also functionally and pin-out compatible with standard DM54LS/DM74LS logic families. The MM54HC05/MM74HC05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

Features

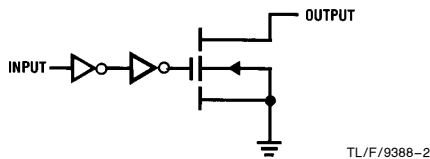
- Open drain for wire-NOR function
- Fanout of 10 LS-TTL loads
- Typical propagation delays:
 t_{PZL} (with 1 k Ω resistor) 8 ns
 t_{PLZ} (with 1 k Ω resistor) 13 ns
- Low input current: 1 μ A maximum

Connection Diagram

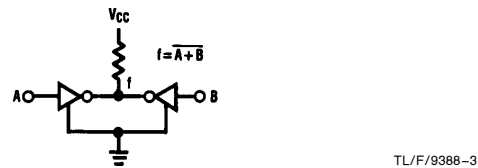


Order Number MM54HC05 or MM74HC05

Logic Diagram



Typical Application



Note: Can be extended to more than 2 inputs.

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK} , I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN} , V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r , t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		74HC	54HC	Units
						T _A = −40°C to +85°C	T _A = −55°C to +125°C	
				Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} I _{OUT} ≤ 20 μA R _L = ∞	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V _{IN} = V _{IH} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I _{LKG}	Maximum High Level Output Leakage Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC}	6.0V		0.5	5	10	μA
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic “N” package: −12 mW/°C from 65°C to 85°C; ceramic “J” package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25^{\circ}C$, $C_L=15\text{ pF}$, $t_r=t_f=6\text{ ns}$

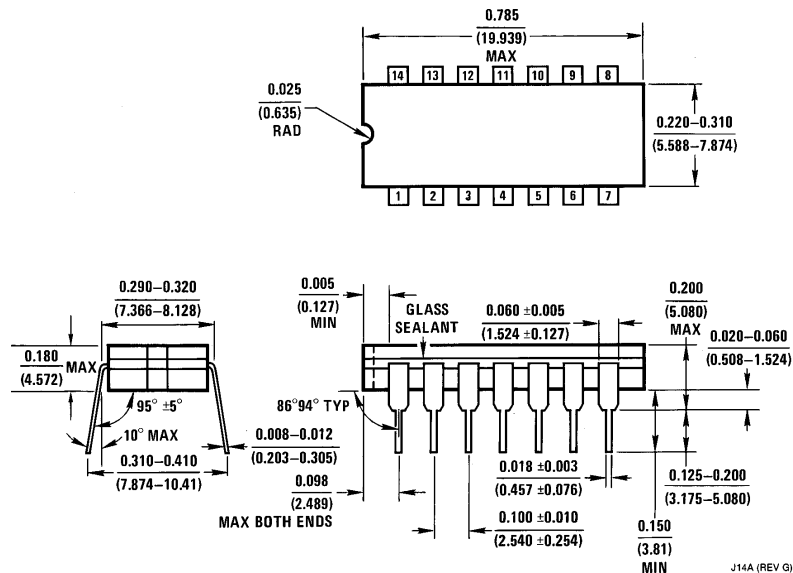
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PZL} , t_{PLZ}	Maximum Propagation Delay	$R_L=1\text{ k}\Omega$	8		ns

AC Electrical Characteristics $V_{CC}=2.0V\text{ to }6.0V$, $C_L=50\text{ pF}$, $t_r=t_f=6\text{ ns}$ unless otherwise specified

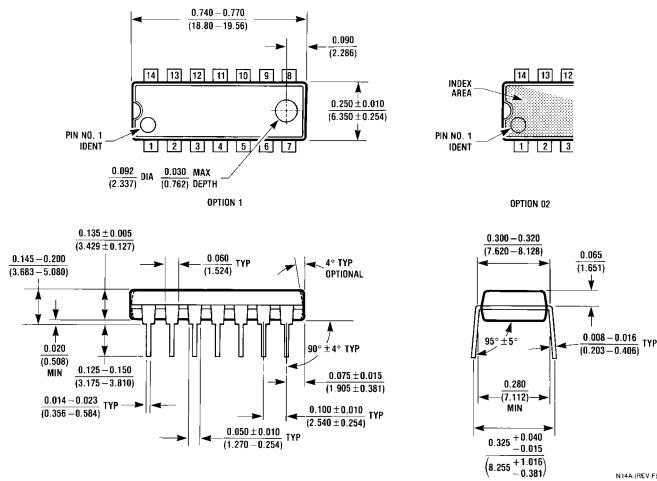
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		74HC T _A = −40°C to +85°C		54HC T _A = −55°C to +125°C		Units
				Typ	Guaranteed Limits					
t _{PZL}	Maximum Propagation Delay	R _L = 1 kΩ	2.0V	30	75	95		110		ns
			4.5V	8	15	19		22		ns
			6.0V	7	13	16		19		ns
t _{PLZ}	Maximum Propagation Delay	R _L = 1 kΩ	2.0V	30	90	115		135		ns
			4.5V	13	18	23		27		ns
			6.0V	12	15	20		23		ns
t _{THL}	Maximum Output Fall Time		2.0V	30	75	95		110		ns
			4.5V	8	15	19		22		ns
			6.0V	7	13	16		19		ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		8						pF
C _{IN}	Maximum Input Capacitance			5	10	10		10		pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD} V_{CC} f + I_{CC}$. The power dissipated by R_L is not included.

Physical Dimensions inches (millimeters)



Order Number MM54HC05J or MM74HC05J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

Order Number MM74HC05N
NS Package Number N14A

N14A (REV F)

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